Remarks

Applicant and his representatives wish to thank Examiner Sullivan and Supervisory Primary Examiner Huff for the very helpful and courteous discussion held on November 7, 2007. The claims have been amended as discussed. The following remarks shall further summarize and expand upon topics discussed.

The present invention relates to a method for forming a metal line. The method (as set forth in amended Claim 1 above) generally comprises:

a) stacking a lower insulating layer, a lower metal layer and an upper insulating layer;

b) patterning a first photosensitive film on the upper insulating layer;

c) using the patterned first photosensitive film as a mask, etching the upper insulating layer until at least a portion of the lower metal layer is exposed;

d) filling an etched portion of the upper insulating layer with a nitride film;

e) patterning a second photosensitive film over the lower metal layer and the nitride film;

f) using the second photosensitive film as a mask, etching the lower metal layer until the lower insulating layer is exposed to form a lower metal line pattern;

g) depositing an IMD (Inter Metal Dielectric) layer on the lower metal line pattern, including the sidewalls of the lower metal line pattern, the lower insulating layer, and the nitride film, thereby forming an air gap within the IMD layer between lines in the lower metal line pattern;

h) planarizing the IMD layer to expose the nitride film;

i) removing the nitride film, thereby forming a contact hole in the IMD layer exposing an upper surface of the lower metal line pattern;

j) filling the contact hole with a conductive material; and

k) depositing an upper metal line over the conductive material.

The references cited against the claims (Furukawa et al, U.S. Pat. No. 6,221,704 [hereinafter "Furukawa"], Wang, U.S. Pat. No. 6,159,840 [hereinafter "Wang"], Grill et al., U.S. Pat. No. 6,737,725 [hereinafter "Grill"], Gardner et al., U.S. Pat. No. 5,869,379 [hereinafter "Gardner"]), and Yasushi, JP 2-047840 [hereinafter "Yasushi"]), neither disclose nor suggest depositing an IMD layer on a lower metal line pattern (including the sidewalls of the lower metal line pattern), the lower insulating layer, and the nitride film, thereby forming an air gap in the IMD layer between lines in the lower metal line pattern (see amended Claim 1 above). Consequently, the present claims are patentable over the cited references.

The Rejection of Claims 1-5 under 35 U.S.C. § 103(a)

The rejection of Claims 1-5 under 35 U.S.C. § 103(a) as being unpatentable over Furukawa and Wang, in view of Grill and Gardner is respectfully traversed.

Furukawa discloses a process for fabricating a short channel field effect transistor with a highly conductive gate (Title). As noted in the final Office Action, Furukawa teaches forming second conductive layer 27 on the first conductive-forming layer 4 (col. 7, ll. 54-56, and FIG. 5). Suitable conductive materials 27 include tungsten, tungsten silicide, titanium silicide, cobalt silicide and titanium nitride (col. 7, ll. 57-59). Only one of the suitable materials is a metal (tungsten); the remaining examples are metal compounds. As will be explained later, under the processing conditions disclosed by Furukawa, even that one example of a metal layer is converted to a metal compound prior to deposition of the insulator layer in which contact holes are formed.

Significantly, as the conductive forming layer 4, Furukawa discloses only doped polysilicon or intrinsic polysilicon with doping ions implanted into it (col. 3, ll. 42-59, and FIGS. 1-3). To one of ordinary skill in the art, this identifies the stacked structures 3/4/7 and 3/4/27/28 of Furukawa as a ***polysilicon*** line or polycide layer, rather than a metal line or metal layer (see Wolf, *Microchip Manufacturing*, Lattice Press, Sunset Beach, California [2004], pp. 54-55 and

60-67; and Wolf et al., *Silicon Processing for the VLSI Era*, vol. 1, Lattice Press, Sunset Beach, California [2000], pp. 723-724, submitted herewith). This distinction is important, in that one of ordinary skill in the art would not necessarily apply a process or technique used in forming a poly layer to a method of forming a metal layer, or vice versa. In fact, Furukawa distinguishes metal lines M1 from the gate (poly) layer structures 3/4/7 and 3/4/27/28 (see, e.g., col. 7, ll. 47-49 and col. 9, ll. 1-7).

Thus, Furukawa does not disclose stacking a lower insulating layer, ***a lower metal line*** and an upper insulating layer, as recited in Claim 1. (It is noted for the record that Furukawa heats the wafer to drive dopant from a dopant source into the polysilicon gate and S/D extension regions; see col. 8, ll. 40-47. At typical dopant drive-in times and temperatures [see *Wolf*, p. 62], any metal 27 deposited on polysilicon gate layer 4 in Furukawa may be expected to form silicide [see *Wolf*, p. 63], which raises a further question about whether Furukawa discloses a stacked lower insulating layer, lower ***metal*** line and upper insulating layer, at least where one would remove the nitride film to form a contact hole exposing an upper surface of the lower metal line.)

Furthermore, Furukawa does not show *adjacent* stacked gate structures 3/4/27/28, presumably because they are too far apart to be shown on the scale of the drawings in Furukawa. Thus, one of ordinary skill in the art would not necessarily conclude that forming an air gap between adjacent stacked gate structures is even possible, much less desirable. However, assuming for the sake of argument that it might be possible, one of ordinary skill in the art would recognize that altering the process of Furukawa to require forming an air gap between adjacent stacked gate structures 3/4/27/28 could have catastrophic consequences. The contacts CA (and thus the corresponding contact holes) in FIGS. 4 and 8 of Furukawa would have to be formed in the same space (i.e., between adjacent stacked gate structures). If the contact hole overlaps the air gap, it would be challenging to reliably form uniform contacts CA.

For example, if an air gap is formed in the dielectric layer between adjacent polysilicon gates, the opening of the subsequently formed contact hole could be smaller than the combined width of the contact hole and the air gap, in which case the opening to the contact hole could close before the combined contact hole and air gap was filled with contact-forming material (see

Wolf et al., *Silicon Processing for the VLSI Era*, vol. 1, Lattice Press, Sunset Beach, California [2000], pp. 210-211 and 217, submitted with the Amendment after final filed September 13, 2007, which respectively show phenomena resulting in voids when a metal deposited into a trench or contact hole by CVD [Fig. 6-47] or sputtering [Fig. 6-53] closes or begins to close at the opening before the contact hole is completely filled). A relatively small contact hole opening would be expected to result in voids in the metal contacts (see *Wolf et al.*, p. 211), which would be expected to significantly affect the uniformity of contact resistance, and thus, have an adverse impact on yield. Thus, one of ordinary skill in the art would not be at all motivated to modify the process or structure of Furukawa to include an air gap between conductive polysilicon gate structures, nor would one of ordinary skill in the art be at all motivated to substitute the stacked gate structures 3/4/27/28 of Furukawa for a stacked lower insulating layer, lower metal line and upper insulating layer typical of metallization layers.

As a result, the disclosure of Furukawa is deficient with regard to (and is arguably essentially irrelevant to) the presently claimed method. At the very least, Furukawa neither discloses nor suggests depositing an IMD layer on a lower metal line pattern (including the sidewalls of the lower metal line pattern), the lower insulating layer, and the nitride film, thereby forming an air gap within the IMD layer between lines in the lower metal line pattern. The remaining cited references fail to cure this deficiency. As a result, no possible combination of cited references can disclose or suggest all of the limitations of Claim 1.

Wang discloses forming a metal layer 202 on the substrate 200 as the bottom layered conductive line of the metal interconnect (col. 2, ll. 49-51 and FIGS. 1 and 2A). A dielectric layer 204 is further formed covering the metal layer 202 and the substrate 200, and thereafter, a stop layer 206 is formed on the dielectric layer 204 (for example, a silicon nitride layer; see col. 2, ll. 51-57 of Wang). A dielectric layer 208 (for example, an oxide layer) is further formed on the stop layer 206 (col. 2, ll. 57-59 of Wang).

Wang then teaches defining the dielectric layer 208, the stop layer 206 and the dielectric layer 204 using a photoresist layer 210, followed by removing the portions of the dielectric layer 208, the stop layer 206 and the dielectric layer 204 not covered by the photoresist layer 210 to

form a via opening 212a and an opening 212b where the air-gap is to be formed (col. 2, ll. 60-67 and FIGS. 1 and 2B). Wang then forms a dielectric material 214 (such as a PECVD oxide layer) on the dielectric layer 208 (col. 3, ll. 7-9 and FIG. 2C). The recipe for forming the dielectric material 214 is adjusted during the deposition process to result in a dielectric material 214 with a slightly inferior step coverage property. The dielectric material 214 thus directly covers the dielectric layer 208, sealing the opening 212b (as in FIG. 2B) to form an air gap 213, but not completely filling the opening 212b (col. 3, ll. 10-15 of Wang). Furthermore, the dielectric material 214 also covers the via opening 212a, resulting in a part of the dielectric material 214 partially filling the via opening 212a. The height of the dielectric material 214 in the via opening 212a and the opening 212b is controlled to be above the stop layer 206, which is favorable in forming the air-gap 213 and manufacturing the via plug (col. 3, ll. 15-22 of Wang).

Wang then forms a photoresist layer 216 on the dielectric material 214, and forms a trench 218 in the dielectric material 214 and the dielectric layer 208 (see FIGS. 2D-2E and col. 3, ll. 23-27 of Wang). The trench 218 is formed by anisotropic etching of the dielectrics 214 and 208 using the stop layer 206 as an etch-stop. The dielectric material 214 and the dielectric layer 208 are completely removed in the via opening 212a to expose the metal layer 202. On the other hand, the dielectric material 214 above the air-gap 213, protected by the photoresist layer 216, remains (col. 3, ll. 27-37 and FIG. 2E of Wang).

Thus, like Furukawa, Wang fails to etch ***the lower metal line*** using the second photosensitive film as a mask. Thus, it is irrelevant whether Wang etches dielectric materials or exposes the lower metal layer by etching using the second photosensitive film as a mask. Wang fails to cure this deficiency of Furukawa with regard to the present Claim 1.

Furthermore, like Furukawa, Wang neither discloses nor suggests depositing an IMD layer on a lower metal line pattern, ***including the sidewalls of the lower metal line pattern***, ***the lower insulating layer***, and the nitride film, thereby forming an air gap within the IMD layer between lines in the lower metal line pattern. The air gap 213 in Wang is formed in dielectric layers 204 and 208 (FIG. 2B), or between dielectric layer 214 and substrate 200 (FIG. 2C), by deposition of dielectric layer 214. (Stop layer 206 of Wang corresponds to the present nitride

layer.) Thus, to the extent that depositing dielectric layer 214 forms air gap 213, the air gap 213 is not in dielectric layer 214, but in one or more other dielectric layers, or between dielectric layer 214 and another structure. Thus, Wang fails to cure this deficiency of Furukawa with regard to the present Claim 1. The remaining cited references (Grill and Gardner) also fail to cure this deficiency, and as a result, no possible combination of cited references can disclose or suggest all of the limitations of Claim 1.

Grill discloses a method for forming a multilayer interconnect structure that includes interconnected conductive wiring and vias spaced apart by a combination of solid or gaseous dielectrics (Abstract, ll. 1-4). The method includes the steps of: (a) forming a first planar via plus line level pair embedded in a dielectric matrix formed from one or more solid dielectrics, wherein at least one of said solid dielectrics is at least partially sacrificial; (b) etching back sacrificial portions of the sacrificial dielectrics to leave cavities extending into and through the via level, while leaving at least some of the original via level dielectric as a permanent dielectric under the lines; (c) partially filling or overfilling the cavities with a place-holder material; (d) planarizing the structure by removing overfill of the place-holder material; (e) repeating steps (a)-(d) as necessary; (f) forming a dielectric bridge layer over the planar structure; and (g) forming air gaps by at least partially extracting the place-holder material (Abstract, ll. 4-end).

Grill teaches that the structure of FIG. 1G (containing wiring structures 185) is overfilled with a sacrificial place-holder (SPH) material 220 to form the structure of FIG. 1H (col. 6, ll. 20-45). It is preferred that the SPH be a material that "gap fills" in a way ***that does not leave cavities*** that will be opened when the SPH is planarized (col. 6, ll. 50-53; emphasis added). After forming the desired number of wiring and via levels (i.e., patterned conductors embedded in a dielectric matrix comprising permanent dielectric materials and SPH materials; see col. 7, ll. 1-5 and FIG. 1L), dielectric bridge layer 250 is formed and patterned with small openings (holes or perforations) 260 to produce the structure of FIG. 1M (see col. 7, ll. 5-7 of Grill). SPH material 220' and 220 in FIG. 1M is then extracted to form the structure of FIG. 1N, with air gaps 270 (col. 7, ll. 35-36).

Thus, like Furukawa and Wang, Grill fails to disclose or suggest depositing an IMD layer on a lower metal line pattern, ***including the sidewalls of the lower metal line pattern***, ***the lower insulating layer***, and the nitride film, thereby forming an air gap within the IMD layer between lines in the lower metal line pattern. As a result, Grill fails to cure this deficiency of Furukawa and Wang with regard to the method recited in Claim 1.

Like Furukawa, Gardner discloses a process for forming a transistor (Abstract, l. 1). As is discussed in *Wolf* and *Wolf et al.*, formation of a transistor occurs at or below the polysilicon level in a CMOS integrated circuit. As a result, the teachings of Gardner may not have much (if any) bearing on the present method, which begins by stacking a lower insulating layer, a lower ***metal*** line and an upper insulating layer.

Gardner teaches that an isotropic etch may be performed on exposed lateral surfaces of ***polysilicon gate conductors 18*** such that the gate conductors are selectively narrowed to a pre-determined lateral thickness (see col. 5, ll. 46-49 and FIG. 6). While masking structures 20 are preferably composed of nitride, they may comprise oxide, silicon oxynitride, or a metal. Thus, depending on whether masking structures 20 are nitride or a metal, Gardner discloses either filling an etched portion of the upper insulating layer with a nitride film **or** stacking a lower insulating layer, a lower metal line and an upper insulating layer. It appears that Gardner cannot disclose both.

Like Furukawa, Gardner teaches removing select portions of polysilicon layer 14 and masking layer 16 to form a gate conductor 18 with overlying masking structure 20 using optical lithography and a dry plasma etch technique (see col. 5, ll. 31-38 and FIG. 4). Thereafter, Gardner discloses that an isotropic etch may be performed on exposed lateral surfaces of polysilicon gate conductors 18 such that the gate conductors are selectively narrowed to a pre-determined lateral thickness (col. 5, ll. 46-49 and FIG. 6). The isotropic etch technique preferably involves using a wet etchant that exhibits high selectivity for polysilicon such that gate conductors 18 may be etched without significant etching of the overlying masking structures 20 (col. 5, ll. 49-53), thereby indicating to one of ordinary skill in the art that masking structure 20 is used as the mask for the isotropic etch of polysilicon gate conductors 18.

After further processing, Gardner teaches that an interlevel dielectric 38 may be CVD deposited from, e.g., a TEOS source across exposed surfaces of the semiconductor topography (col. 6, l. 66-col. 7, l. 1 and FIG. 11). The presence of masking structures 20 above gate conductors 18 may prevent the accumulation of dielectric material upon the sidewall surfaces of gate conductors 18. As a result, air gaps 40 may be formed laterally ***adjacent to gate conductors 18*** underneath the masking structures 20 (col. 7, ll. 1-6; emphasis added). Thus, Gardner deposits a dielectric material such that air gaps are formed ***between*** the dielectric material and polysilicon gate conductors 18, rather than ***in*** the dielectric material, between lines in the lower metal line pattern.

Thus, like Furukawa, Wang and Grill, Gardner fails to disclose or suggest depositing an IMD layer on a lower metal line pattern, ***including the sidewalls of the lower metal line pattern***, ***the lower insulating layer***, and the nitride film (recall that masking structures 20 can be ***either*** metal ***or*** a nitride, not both), thereby forming an air gap in the IMD layer between lines in the lower metal line pattern. As a result, Gardner fails to cure this deficiency of Furukawa, Wang and Grill with regard to the method recited in Claim 1.

As a result, no possible combination of the cited references discloses or suggests depositing an IMD layer on a lower metal line pattern, ***including the sidewalls of the lower metal line pattern***, ***the lower insulating layer***, and the nitride film, thereby forming an air gap in the IMD layer between lines in the lower metal line pattern, as recited in Claim 1 above. Consequently, this ground of rejection is unsustainable, and should be withdrawn.

The Rejection of Claim 8 under 35 U.S.C. § 103(a)

The rejection of Claim 8 under 35 U.S.C. § 103(a) is respectfully traversed.

Claim 8 depends from Claim 1, and thus contains all of the limitations of Claim 1. As mentioned above, the combination of Furukawa, Wang, Grill and Gardner is deficient with regard to depositing an IMD layer on the lower metal line pattern (including the sidewalls of the

lower metal line pattern), the lower insulating layer, and a nitride film thereon, ***thereby forming an air gap*** in the IMD layer between lines in the lower metal line pattern, as recited in Claim 1. Yasushi fails to cure these deficiencies.

Although Yasushi discloses removing a nitride layer by wet etching, Yasushi appears to be silent with regard to depositing an IMD layer on the lower metal line pattern (including the sidewalls thereof), a lower insulating layer, and a nitride film on the lower metal line pattern, thereby forming an air gap in the IMD layer between lines in the lower metal line pattern, as recited in Claim 1. Thus, for at least the same reasons as set forth above for Claim 1, Claim 8 is patentable over the combination of Furukawa, Wang, Grill, Gardner and Yasushi. Accordingly, this ground of rejection is unsustainable, and should be withdrawn.

Conclusions

In view of the above amendments and remarks, all bases for objection and rejection are overcome, and the application is in condition for allowance. Early notice to that effect is earnestly requested.

If it is deemed helpful or beneficial to the efficient prosecution of the present application, the Examiner is invited to contact Applicant's undersigned representative by telephone.

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